a low compression rate, the spatial frequency information may be determined using the correlation between the compression rate and the spatial frequency.

[0162] The spatial frequency information for each channel of the texture may be calculated in real time when performing the texturing operation by the graphics processing unit **100** including the texture processing unit **130**. The controller **131** may obtain the calculated spatial frequency information for each channel from the graphics processing unit **100**.

[0163] The spatial frequency information for each respective channel of the texture may be directly input through an application program executed by the graphics processing unit **100**, which is a non-transitory hardware device.

[0164] In operation S**1220**, the texture processing unit **130** may determine a filtering control signal for each respective channel of the texture based on the spatial frequency information for each channel.

[0165] The texture processing unit **130** may determine the filtering control signal independently for each channel when the spatial frequencies of the channels included in the spatial frequency information for respective channels are different from each other. The texture processing unit **130** may determine the filtering control signal for each channel so that anti-aliasing filtering based on the spatial frequency of the channel is performed on a channel satisfying the predetermined condition in which an aliasing phenomenon occurs. The filtering control signal for each channel may include a control signal for each channel for the anti-aliasing filtering. The filtering control signal for each channel may further include the control signal for each respective channel for a filtering mode requested by an application program executed on a non-transitory hardware device, as well as the control signal for each channel for the anti-aliasing filtering.

[0166] FIG. **13** is a detailed flowchart for describing an operation of determining a filtering control signal for each channel in a texture processing method according to an embodiment.

[0167] In operation S**1310**, the texture processing unit **130** may obtain a sampling frequency for a texture.

[0168] In operation S**1320**, the texture processing unit **130** may determine a channel having the highest spatial frequency as a reference channel based on the spatial frequency information for each channel.

[0169] In operation S**1330**, the texture processing unit **130** may determine a filtering control signal of the reference channel based on the spatial frequency of the reference channel and the sampling frequency.

[0170] In operation S**1340**, the texture processing unit **130** may compare the spatial frequency of the reference channel and the spatial frequencies of other channels excluding the reference channel, and determine filtering control signals of the other channels excluding the reference channel.

[0171] FIG. **14** is a detailed flowchart describing an operation of determining a filtering control signal for each channel in a texture processing method according to an embodiment.

[0172] In operation S**1410**, the texture processing unit **130** may obtain a sampling frequency for a texture.

[0173] In operation S**1420**, the texture processing unit **130** may compare the spatial frequency for each channel included in spatial frequency information for each channel and the sampling frequency, and determine a filtering control signal for each channel.

[0174] Referring to FIG. **12** again, in operation S**1230**, the texture processing unit **130** may perform filtering for each channel on the texture according to the filtering control signal for each channel.

[0175] The texture processing unit **130** may operate the first filter including anti-aliasing filters corresponding to the channels configuring the texture and the second filter including filters performing filtering according to a filtering mode requested by an application program, for each channel according to the filtering control signal for each channel.

[0176] The apparatuses, units, modules, devices, and other components illustrated in FIGS. **1-14** that perform the operations described herein with respect to FIGS. **1-14** are implemented by hardware components. Examples of hardware components include controllers, sensors, generators, drivers, and any other electronic components known to one of ordinary skill in the art. The hardware components are implemented by one or more processors or computers. A processor or computer is implemented by one or more processing elements, such as an array of logic gates, a controller and an arithmetic logic unit, a digital signal processor, a microcomputer, a programmable logic controller, a field-programmable gate array, a programmable logic array, a microprocessor, or any other device or combination of devices known to one of ordinary skill in the art, upon full understanding of the present disclosure, that is capable of responding to and executing instructions in a defined manner to achieve a desired result. In one example, a processor or computer includes, or is connected to, one or more memories storing instructions or software that are executed by the processor or computer. Hardware components implemented by a processor or computer execute instructions or software, such as an operating system (OS) and one or more software applications that run on the OS, to perform the operations described herein with respect to FIGS. **1-14**. The hardware components also may access, manipulate, process, create, and store data in response to execution of the instructions or software. For simplicity, the singular term "processor" or "computer" may be used in the description of the examples described herein, but in other examples multiple processors or computers are used, or a processor or computer includes multiple processing elements, or multiple types of processing elements, or both. In one example, a hardware component includes multiple processors, and in another example, a hardware component includes a processor and a controller. A hardware component has any one or more of different processing configurations, examples of which include a single processor, independent processors, parallel processors, single-instruction single-data (SISD) multiprocessing, single-instruction multiple-data (SIMD) multiprocessing, multiple-instruction single-data (MISD) multiprocessing, and multiple-instruction multiple-data (MIMD) multiprocessing.

[0177] The methods illustrated in FIGS. **1-14** that perform the operations described herein with respect to FIGS. **1-14** are performed by a processor or a computer as described above executing instructions or software to perform the operations described herein.

[0178] Instructions or software to control a processor or computer to implement the hardware components and perform the methods as described above are written as computer programs, code segments, instructions or any combination thereof, for individually or collectively instructing or configuring the processor or computer to operate as a